IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

First Named Inventor: Douglas L. Youngblood	§	Atty. Docket: INSL.0083
Serial No.: 10/766,197	§	Examiner: ABDULSELAM, ABBAS I
Filed: January 28, 2004	§	CONFIRMATION NO.: 3357
Title: MULTIPLE CHANNEL PROGRAMMABLE GAMMA CORRECTION VOLTAGE GENERATOR	§	Group Art Unit: 2629

APPELLANT'S APPEAL BRIEF

Board of Patent Appeals and Interferences
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Appellant respectfully requests the Board of Patent Appeals and Interferences to reverse the final rejection of claims 1-4, 9-15, and 17-22 under 35 U.S.C. §103(a). The present invention as recited in these claims is not obvious in view of the prior art relied upon by the Examiner.

REAL PARTY IN INTEREST

The real party in interest is Intersil Americas Inc.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-15 and 17-21 are currently pending and claim 16 was previously canceled.

Claims 1-4, 9-15 and 17-22 were rejected and are involved in this appeal.

Claims 5-8 were objected to as depending upon a non-allowed claim but were otherwise considered allowable and are not involved in this appeal.

STATUS OF AMENDMENTS

None of the claims involved in this appeal were amended after Final Rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 recites a multiple channel programmable gamma correction voltage generator (107 of FIG. 1 as described on page 8, line 19 to page 11, line 6, 400 of FIG. 4 as described on page 18, line 6 to page 22, line 15, 500 of FIG. 5 as described on page 22, line 16 to page 25, line 15) comprising a reference voltage (VREF+ and VREF-, described on page 11, lines 11 - 28) applied across a resistor ladder (401 of FIGs 4 and 5, described on page 19, lines 5-29), said resistor ladder including M adjustable tap resistors (RB_1 - RB_M of FIGs 4 and 5, described on page 12, line 28 to page 13, line 26 and on page 18, line 16 to page 19, line 4) distributed along said resistor ladder, each providing a corresponding one of M tap voltages (VS1 - VSM of FIGs 4 and 5, described on page 13, line 27 to page 14, line 20) distributed according to a gamma correction value, wherein M is a positive integer, said resistor ladder comprising a plurality of first resistors coupled in series (RA_1 - RA_{M+1} of FIGs 4 and 5, described on page 19, lines 5-29), each of said plurality of first resistors comprising a plurality of second resistors coupled in series (RA1 including RA1_1 - RA1_Q of FIGs 4 and 5, described on page 19, lines 5-29) forming a plurality of intermediate locations, M buffers (209 of FIGs 2 and 3, described as buffer amplifiers on page 15, lines 3-13), each having an input receiving a corresponding one of said M tap voltages and an output providing a corresponding one of M gamma correction voltages (VOUT1 - VOUTM of FIGs 2 and 3, described on page 15, lines 3-13), select logic (DECODER1 405, switch sets SS1-SSQ of RA1, and switches S_1 - S_{P-1} of FIGs 4 and 5, described on page 13, line 23 to page 14, line 3, page 18, line 19 to page 19, line 1, page 19, line 20 to page 22, line 15; or select logic 603 of FIG. 6, described on page 24, line 14 to page 25, line 15) which inserts each of said M adjustable tap resistors into said resistor ladder into M of said plurality of first resistors by inserting a corresponding one of said M adjust adjustable tap resistors at a selected one of said plurality of intermediate locations of a corresponding one of said plurality of first resistors, and that selects a tap point of each of said M adjustable tap resistors to select each of said M tap voltages based on corresponding select values (SEL1 - SELM of FIGs 4 and 4, described on page 14, lines 3-26 and page 18, lines 12-16), and a programmable non-volatile memory device (MEMORY 207 of FIG. 4, described on page 14, line 21 to page 15, line 2, or MEMORY 305 of FIG. 5 described on page 16, line 26 to page 17,

line 10, or MEMORY 601 of FIG. 6, described on page 24, line 14 to page 25, line 15), coupled to said select logic, that provides said select values indicative of said gamma correction value.

Claim 14 recites an integrated circuit (IC) (page 5, line 13), comprising a resistor ladder (401 of FIGs 4 and 5, described on page 19, lines 5-29) coupled to a reference voltage (VREF+ and VREF-, described on page 11, lines 7 - 28), a plurality of adjustable tap resistors distributed along said resistor ladder (RB_1 - RB_M of FIGs 4 and 5, described on page 12, line 28 to page 13, line 26 and on page 18, line 16 to page 19, line 4) and providing a plurality of selectable tap voltages (VS1 - VSM of FIGs 4 and 5, described on page 13, line 27 to page 14, line 20), a plurality of first resistors distributed along said resistor ladder (RA_1 - RA_{M+1} of FIGs 4 and 5, described on page 19, lines 5-29), each coupled to a corresponding one of said plurality of adjustable tap resistors, each first resistor comprising a plurality of second resistors coupled in series (RA1 including RA1_1 - RA1_Q of FIGs 4 and 5, described on page 19, lines 5-29) forming a plurality of first junctions, and first switch logic (switch sets SS1-SSQ of RA1 and switches S_1 - S_{P-1}, described on page 13, line 23 to page 14, line 3, page 18, line 19 to page 19, line 1, page 19, line 20 to page 22, line 15; or select logic 603 of FIG. 6, described on page 24, line 14 to page 25, line 15) that inserts said corresponding one of said plurality of adjustable tap resistors at one of said plurality of first junctions, a programmable non-volatile memory (MEMORY 207 of FIG. 4, described on page 14, line 21 to page 15, line 2, or MEMORY 305 of FIG. 5 described on page 16, line 26 to page 17, line 10, or MEMORY 601 of FIG. 6, described on page 24, line 14 to page 25, line 15) that stores at least one digital gamma value, select logic (DECODER1 of FIGs 4 and 5, described on page 18, line 27 to page 19, line 4 and page 21, line 25 to page 22, line 15; or select logic 603 of FIG. 6, described on page 24, line 14 to page 25, line 15), coupled to said memory, to said first switch logic and to said plurality of adjustable tap resistors, that controls said first switch logic and that selects each of said selectable tap voltages according to said at least one digital gamma value, and a plurality of buffers (209 of FIGs 2 and 3, described as buffer amplifiers on page 15, lines 3-13) having inputs receiving selected tap voltages and outputs that provide a plurality of gamma correction voltages (VOUT1 - VOUTM of FIGs 2 and 3, described on page 15, lines 3-13).

Claim 19 recites an imaging system (FIG. 1, display system 100 described beginning page 8, line 19), comprising an imaging device having a gamma factor (LCD PANEL 101 of FIG. 1, described on page 9, line 25 to page 10, line 14), a driver circuit (COLUMN DRIVERS 103 of FIG. 1, described on page 9, lines 8 - 24) that provides a set of DC reference voltages to

said imaging device based on a set of gamma corrected bias voltages (109 of FIG.1, described on page 9, lines 6 - 24), and a programmable gamma correction voltage generator (107 of FIG. 1 as described on page 8, line 19 to page 11, line 6, 400 of FIG. 4 as described on page 18, line 6 to page 22, line 15, 500 of FIG. 5 as described on page 22, line 16 to page 25, line 15) that provides said set of gamma corrected bias voltages configured to compensate for said gamma factor, said programmable gamma correction voltage generator comprising a reference voltage (VREF+ and VREF-, described on page 11, lines 11 - 28) coupled across a resistor ladder (401 of FIGs 4 and 5, described on page 19, lines 5-29) comprising a plurality of resistors coupled in series and forming a plurality of intermediate junctions, a plurality of potentiometers (RB_1 - RB_M of FIGs 4 and 5, described on page 12, line 28 to page 13, line 26 and on page 18, line 16 to page 19, line 4) distributed along said resistor ladder and providing a plurality of variable tap voltages (VS1 - VSM of FIGs 4 and 5, described on page 13, line 27 to page 14, line 20), wherein each of said plurality of potentiometers is inserted at a corresponding one of said plurality of intermediate junctions, a programmable non-volatile memory (MEMORY 207 of FIG. 4, described on page 14, line 21 to page 15, line 2, or MEMORY 305 of FIG. 5 described on page 16, line 26 to page 17, line 10, or MEMORY 601 of FIG. 6, described on page 24, line 14 to page 25, line 15) that stores at least one digital gamma value, select logic (DECODER1 405, switch sets SS1-SSQ of RA1, and switches S_1 - S_{P-1} of FIGs 4 and 5, described on page 13, line 23 to page 14, line 3, page 18, line 19 to page 19, line 1, page 19, line 20 to page 22, line 15; or select logic 603 of FIG. 6, described on page 24, line 14 to page 25, line 15), coupled to said memory and to said plurality of potentiometers, that selects from among said plurality of intermediate junctions for inserting said plurality of potentiometers and that selects each of said variable tap voltages according to said digital gamma value, and a plurality of buffers (209 of FIGs 2 and 3, described as buffer amplifiers on page 15, lines 3-13) having inputs receiving selected tap voltages and outputs that provide said set of gamma corrected bias voltages (VOUT1 - VOUTM of FIGs 2 and 3, described on page 15, lines 3-13).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 9-13, and 18-22 are patentable under 35 U.S.C. §103(a) over Kudo et al. (US Pat. No. 7,023,458, hereinafter "Kudo") in view of Kato (US Pub. No. 20020125112, hereinafter "Kato").

Whether claims 2-4, 14-15, and 17 are patentable under 35 U.S.C. §103(a) over Kudo in view of Kato and Suzuki et al. (US Pat. No. 6,157,335, hereinafter "Suzuki").

ARGUMENT

Appellant respectfully traverses the §103(a) rejection of claims 1, 9-13 and 18-22 as being unpatentable over Kudo in view of Kato and asserts that claims 1, 9-13 and 18-22 are allowable over Kudo in view of Kato.

Although the present invention is not limited to the specific embodiments shown and described in the application, a brief description of the embodiments of FIGs 4-6 is now described to ensure an understanding of the claims. As shown in FIG. 4, each resistor RA_1 - RA_{M+1} (first resistors) of the resistor ladder 401 includes multiple resistors (second resistors) coupled in series forming intermediate locations. The resistor RA_1, for example, is shown in an exploded view as resistor RA1 with Q series resistors RA1_1 to RA1_Q and with switch sets SS1 - SSQ (select logic) coupled at respective intermediate locations between each pair of the RA1_X resistors and below the last resistor RA1_Q. The resistor ladder 401 also includes resistors RB_1 - RB_M (adjustable tap resistors) in which the first resistor RB_1 is shown in exploded view as resistor RB1 including P series-coupled resistors RB1_1 to RB1_P. The DECODER1 405 (select logic) asserts the gross select (GS) signal to select one of the switch sets SS1 - SSQ which inserts the resistor RB1 at the corresponding intermediate location of the selected switch set. As shown, for example, the switch set SS1 is selected so that the intermediate location between the resistors RA1_1 and RA1_2 is disconnected (by opening switch 1 of switch set SS1) and the resistor RB1 is inserted between the resistors RA1_1 and RA1_2 (by closing switches 2 and 3 of switch set SS1). It is noted that only one of the switch sets SS1 - SSQ is selected at a time and that one is always selected for each of the first resistors RA_1 - RA_{M+1}. The DECODER1 405 also asserts the fine select (FS) signal to select one of the switches S_1 - S_{P-1} (select logic) to select a corresponding tap point of the adjustable tap resistor RB1. As shown, for example, the switch S_2 is selected to select the tap point between resistors RB1_2 and RB1_3 to control the first tap voltage VS1. The DECODER1 405 receives a signal SEL1 (one of M select values SEL1 - SELM) from MEMORY 207 (programmable non-volatile memory device) to control the GS and FS signals for gamma voltage control. As described in the specification, each of the remaining resistors RA_2 - RA_{M+1} and RB_2 - RB_M is configured in substantially the same manner. Furthermore, corresponding decoders (e.g., DECODER2 - DECODERM, not shown) are

provided as controlled by the select values SEL2 - SELM, respectively, for controlling the GS and FS signals for each resistor combination for determining the voltages of the remaining tap voltages VS2 - VSM, respectively.

Claim 1 is allowable over Kudo in view of Kato, since Kudo in view of Kato does not show a "resistor ladder including M adjustable tap resistors distributed along said resistor ladder, each providing a corresponding one of M tap voltages distributed according to a gamma correction value, wherein M is a positive integer", in which the resistor ladder comprises "a plurality of first resistors coupled in series, each of said plurality of first resistors comprising a plurality of second resistors coupled in series forming a plurality of intermediate locations" and "select logic which inserts each of said M adjustable tap resistors into said resistor ladder into M of said plurality of first resistors by inserting a corresponding one of said M adjust adjustable tap resistors at a selected one of said plurality of intermediate locations of a corresponding one of said plurality of first resistors, and that selects a tap point of each of said M adjustable tap resistors to select each of said M tap voltages based on corresponding select values" as recited in claim 1.

FIG. 3 of Kudo shows the resistance ladder 307, which includes variable resistors 321 to 324 coupled in series with resistive voltage division circuits 326 to 331 (see Kudo description beginning col. 7, line 44). Kudo describes the configuration of the resistive voltage division circuits 326 to 331 in FIGs 7A and 7B as described beginning col. 13, line 25 (it is noted that there does not appear to be FIGS. 7E and 7C as stated therein). As shown and described in FIG. 7A of Kudo, the fixed resistors 1R are not selectively inserted but instead are fixed within the resistance ladder 307 of FIG. 3. As shown and described in Kudo, the circuits 701 and 703 are controlled to select one of the "micro adjustment gray scale voltages A to H" (Kudo, col. 13, lines 30-36) by selecting one of the junctions at A-H. Such configuration of Kudo does not show select logic which inserts each of M adjustable tap resistors into a resistor ladder into M of a plurality of first resistors by inserting a corresponding one of the M adjust adjustable tap resistors at a selected one of a plurality of intermediate locations of a corresponding one of the plurality of first resistors as recited in claim 1. Although Kudo shows selecting taps of a resistive ladder, Kudo does not show inserting adjustable tap resistors at selected junctions of a resistor ladder as recited in claim 1.

Kudo FIGs 4A - 4C show and describe an embodiment of the variable resistances 321 - 324 of the resistor ladder 307 of Kudo, in which any one or more of the resistors 4R, 8R and 16R

are selectively included within the resistor ladder 307 or otherwise excluded by closing a corresponding switch 403 - 405. The resistors 4R, 8R and 16R of each variable resistance of Kudo are not selectively inserted at a selected intermediate location of a plurality of first resistors as claimed but are simply selectively bypassed. Furthermore, the resistors 4R, 8R and 16R of each variable resistance of Kudo are not adjustable tap resistors as recited in claim 1. As recited in claim 1, each of the M adjustable tap resistors provides a tap voltage whereas the resistors 4R, 8R and 16R do not provide a tap voltage. In this manner, the resistors 4R, 8R and 16R of Kudo are not adjustable tap resistors and are not inserted at a selected one of a plurality of intermediate locations of a corresponding one of the plurality of first resistors as recited in claim 1.

It was stated in the "Response to Arguments" section on page 8 of the Final Office Action that Kudo shows each first resistor (326-330) comprising a plurality of second resistors (308-313) coupled in series forming a plurality of first junctions. The circuits 308-313 of Kudo, however, are not resistors but instead are "selector circuits" (Kudo, col. 8, lines 59 - 67). The selector circuits 308-313 are described in Kudo with more particularity in FIGS 7A and 7B in which the internal configuration of "one of the selector circuits" is shown as selector circuit 701 (Kudo, col. 13, lines 25-30). Selector circuit 701 as shown in FIG. 7A of Kudo does not include resistors but instead comprises selector group circuits 704, 705 and 706 controlled by register setting circuit 703. The selector group circuits 704, 705 and 706 are switches for selecting between tap points A-H of a resistive divider circuit 702. The selector circuits 308-313, therefore, are not resistors but are switches for selecting tap voltages of a fixed resistor string.

Kato also does not show a "resistor ladder including M adjustable tap resistors distributed along said resistor ladder, each providing a corresponding one of M tap voltages distributed according to a gamma correction value, wherein M is a positive integer", in which the resistor ladder comprises "a plurality of first resistors coupled in series, each of said plurality of first resistors comprising a plurality of second resistors coupled in series forming a plurality of intermediate locations" and "select logic which inserts each of said M adjustable tap resistors into said resistor ladder into M of said plurality of first resistors by inserting a corresponding one of said M adjust adjustable tap resistors at a selected one of said plurality of intermediate locations of a corresponding one of said plurality of first resistors, and that selects a tap point of each of said M adjustable tap resistors to select each of said M tap voltages based on

corresponding select values" as recited in claim 1. And any reasonable combination of Kudo and Kato fails to meet the limitations of claim 1.

As shown in FIGs 2, 3 and 5 and as described in paragraphs 31, 32 and 71 of Kato, the adjustment resistor string 21 includes a plurality of resistors Ra1 - Rax+1 connected in series, in which each of the resistors have resistances substantially equal to each other to equally divide the voltage between VCC and VSS. As described in paragraph 71 of Kato, γ-correction voltages may include three or more voltages which are applied to one or more taps of the γ-correction resistor string 41 in addition to both the ends thereof. While such enables adjustment of a higher voltage side or a lower voltage side to improve the accuracy of the adjustment, such has nothing to do with inserting a corresponding one of said M adjust adjustable tap resistors at a selected one of a plurality of intermediate locations of a corresponding one of a plurality of first resistors as recited in claim 1.

Appellant respectfully submits, therefore, that claim 1 is allowable over Kudo in view of Kato. Claims 8-13 are allowable as depending upon allowable claim 1. Appellant requests withdrawal of this rejection and allowance of claims 1 and 8-13.

Claim 19 is allowable over Kudo in view of Kato for similar reasons. Kudo in view of Kato does not show a programmable gamma correction voltage generator including "a reference voltage coupled across a resistor ladder comprising a plurality of resistors coupled in series and forming a plurality of intermediate junctions", "a plurality of potentiometers distributed along said resistor ladder and providing a plurality of variable tap voltages, wherein each of said plurality of potentiometers is inserted at a corresponding one of said plurality of intermediate junctions", and "select logic" which "selects from among said plurality of intermediate junctions for inserting said plurality of potentiometers and that selects each of said variable tap voltages according to said digital gamma value" as recited in claim 19. In a similar manner as previously described, Kudo in view of Kato does not show selectively inserting potentiometers at selected junctions within a resistor ladder in which the potentiometers provide variable tap voltages as recited in claim 19.

Appellant respectfully submits, therefore, that claim 19 is allowable over Kudo in view of Kato. Claims 20-22 are allowable as depending upon an allowable base claim. Appellant requests withdrawal of this rejection and allowance of claims 19-22.

It is noted that claim 18 was rejected based on Kudo in view of Kato whereas claim 14, from which claim 18 depends, was not. Nonetheless, claim 14 is allowable over Kudo in view of

Kato for similar reasons recited above with respect to claim 1. Claim 14 recites a resistor ladder, a plurality of adjustable tap resistors distributed along the resistor ladder and providing a plurality of selectable tap voltages, and a plurality of first resistors distributed along the resistor ladder. Each first resistor is coupled to a corresponding one of the plurality of adjustable tap resistors, in which each first resistor comprises a plurality of second resistors and first switch logic. The second resistors are coupled in series forming a plurality of first junctions, and the first switch logic inserts a corresponding one of the plurality of adjustable tap resistors at one of the plurality of first junctions. Stated another way, the resistor ladder comprises a plurality of second resistors (grouped as "first resistors"), where the second resistors are coupled in series forming a plurality of first junctions, in which each of the adjustable tap resistors is inserted by the first switch logic into the first junctions.

Kudo in view of Kato does not show a resistor ladder comprising adjustable tap resistors which are inserted into selected junctions (as controlled by select logic) as recited in claim 14, so that claim 14 is allowable over Kudo in view of Kato. Suzuki does not overcome the deficiencies of Kudo in view of Kato, so that claim 14 is allowable over Kudo in view of Kato and Suzuki. Claim 18 is allowable as depending upon allowable claim 14. Appellant requests withdrawal of this rejection of claim 18 and allowance of claim 18.

Appellant respectfully traverses the §103(a) rejection of claims 2-4, 14-15 and 17 as being unpatentable over Kudo in view of Kato and Suzuki.

Suzuki does not overcome the deficiencies of Kudo in view of Kato with respect to claim 1, so that claims 2-4 are allowable as depending upon allowable claim 1. Likewise, and as previously noted, Suzuki does not overcome the deficiencies of Kudo in view of Kato with respect to claim 14, so that claims 15 and 17 are also allowable as depending upon allowable claim 14. Appellant requests withdrawal of this rejection and allowance of the claims 2-4, 14-15 and 17.

CONCLUSION

Accordingly, Appellant respectfully submits that claims 1, 9-13, and 18-22 are allowable over Kudo in view of Kato, and that claims 2-4, 14-15, and 17 are allowable over Kudo in view of Kato and Suzuki. Appellant therefore requests that the Board overturn the rejections of the claims involved in this Appeal and that these claims be allowed and the patent passed to issuance.

Respectfully submitted,

Date: June 20, 2008

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CLAIMS APPENDIX

APPLICATION CLAIMS INVOLVED IN THIS APPEAL

1. A multiple channel programmable gamma correction voltage generator, comprising:

a reference voltage applied across a resistor ladder;

said resistor ladder including M adjustable tap resistors distributed along said resistor ladder, each providing a corresponding one of M tap voltages distributed according to a gamma correction value, wherein M is a positive integer;

said resistor ladder comprising a plurality of first resistors coupled in series, each of said plurality of first resistors comprising a plurality of second resistors coupled in series forming a plurality of intermediate locations;

M buffers, each having an input receiving a corresponding one of said M tap voltages and an output providing a corresponding one of M gamma correction voltages;

select logic which inserts each of said M adjustable tap resistors into said resistor ladder into M of said plurality of first resistors by inserting a corresponding one of said M adjust adjustable tap resistors at a selected one of said plurality of intermediate locations of a corresponding one of said plurality of first resistors, and that selects a tap point of each of said M adjustable tap resistors to select each of said M tap voltages based on corresponding select values; and

a programmable non-volatile memory device, coupled to said select logic, that provides said select values indicative of said gamma correction value.

2. The multiple channel programmable gamma correction voltage generator of claim 1, wherein:

each of said M adjustable tap resistors comprises P resistors coupled in series forming P-1 intermediate junctions, wherein P is a positive integer; and

wherein said select logic comprises P-1 switches, each having a first terminal coupled to a corresponding one of said P-1 intermediate junctions and a second terminal coupled to a common tap node providing a corresponding one of said M tap voltages.

3. The multiple channel programmable gamma correction voltage generator of claim 2, wherein said select logic includes decoder logic which closes one of said P-1 switches of each of said M adjustable tap resistors to select each of said M tap voltages based on a corresponding one of M select values from said memory device.

4. The multiple channel programmable gamma correction voltage generator of claim 3, wherein said decoder logic comprises M decoders, each receiving a corresponding one of said M select values and selecting a corresponding one of said P-1 switches of a corresponding one of said M adjustable tap resistors.

5. The multiple channel programmable gamma correction voltage generator of claim 1, wherein:

said plurality of first resistors includes M+1 first resistors evenly distributed along said resistor ladder forming M intermediate locations;

wherein at least M of said first resistors each comprise Q second resistors coupled in series forming Q-1 intermediate locations and an end location, wherein Q is a positive integer;

wherein said select logic comprises Q switch sets, each coupled between a respective pair of said second resistors at a corresponding one of said Q intermediate locations and said end location; and

wherein each of said switch sets is operative, when selected, to decouple said Q second resistors at a corresponding one of said Q-1 intermediate locations and said end location and to insert a corresponding one of said M adjustable tap resistors.

6. The multiple channel programmable gamma correction voltage generator of claim 5, further comprising:

each of said M adjustable tap resistors comprising P third resistors coupled in series forming P-1 intermediate junctions, wherein P is a positive integer; and

said select logic comprising P-1 switches, each having a first terminal coupled to a corresponding one of said P-1 intermediate junctions and a second terminal coupled to a common tap node providing a corresponding one of said M tap voltages.

7. The multiple channel programmable gamma correction voltage generator of claim 6, wherein said memory device asserts first signals to select from among said switch sets of each said first resistor for gross adjustment and asserts second signals to select from among said switches of each of said M adjustable tap resistors for fine adjustment.

8. The multiple channel programmable gamma correction voltage generator of claim 6, wherein said select logic comprises decoder logic which provides a set of M gross adjustment values and provides a set of M fine adjustment values to select each of said M tap voltages based on a corresponding one of said M select values, wherein each said gross adjustment value selects a corresponding one of said switch sets, and wherein each fine adjustment value selects a corresponding one of said switches.

9. The multiple channel programmable gamma correction voltage generator of claim 1, further comprising a set of latches with an external load coupled to said memory device and providing said select values to said select logic.

10. The multiple channel programmable gamma correction voltage generator of claim 9, wherein said memory device stores a plurality of sets of select values, each corresponding to a different gamma correction value, and wherein said memory device includes an address control input for selecting from among said plurality of sets of select values and loading said set of latches.

11. The multiple channel programmable gamma correction voltage generator of claim 1, wherein said resistor ladder is incorporated into a single integrated circuit (IC).

12. The multiple channel programmable gamma correction voltage generator of claim 11, wherein said buffers, select logic and memory device are incorporated into said IC.

13. The multiple channel programmable gamma correction voltage generator of claim 1, wherein each of said M buffers comprises an operational amplifier configured as a voltage follower.

14. An integrated circuit (IC), comprising:

a resistor ladder coupled to a reference voltage;

a plurality of adjustable tap resistors distributed along said resistor ladder and providing a plurality of selectable tap voltages;

a plurality of first resistors distributed along said resistor ladder, each coupled to a corresponding one of said plurality of adjustable tap resistors, each first resistor comprising:

a plurality of second resistors coupled in series forming a plurality of first junctions; and

first switch logic that inserts said corresponding one of said plurality of adjustable tap resistors at one of said plurality of first junctions;

a programmable non-volatile memory that stores at least one digital gamma value;

select logic, coupled to said memory, to said first switch logic and to said plurality of adjustable tap resistors, that controls said first switch logic and that selects each of said selectable tap voltages according to said at least one digital gamma value; and

a plurality of buffers having inputs receiving selected tap voltages and outputs that provide a plurality of gamma correction voltages.

15. The IC of claim 14, wherein each of said plurality of adjustable tap resistors comprises:

a plurality of resistors coupled in series and forming a plurality of junctions; and

switch logic that selects one of said plurality of junctions.

17. The IC of claim 14, wherein:

each of said plurality of adjustable tap resistors comprises:

a plurality of third resistors coupled in series and forming a plurality of second junctions; and

second switch logic that selects one of said plurality of second junctions; and

said select logic providing a gross adjustment to each said first switch logic and a fine adjustment to each said second switch logic.

18. The IC of claim 14, further comprising:

a set of latches, coupled to said memory, that enables programming and selection of a plurality of a plurality of digital gamma values in said memory; and

control logic providing address control to said memory for selecting one of said plurality of digital gamma values.

19. An imaging system, comprising:

an imaging device having a gamma factor;

a driver circuit that provides a set of DC reference voltages to said imaging device based on a set of gamma corrected bias voltages; and

a programmable gamma correction voltage generator that provides said set of gamma corrected bias voltages configured to compensate for said gamma factor, said programmable gamma correction voltage generator comprising:

a reference voltage coupled across a resistor ladder comprising a plurality of resistors coupled in series and forming a plurality of intermediate junctions;

a plurality of potentiometers distributed along said resistor ladder and providing a plurality of variable tap voltages, wherein each of said plurality of potentiometers is inserted at a corresponding one of said plurality of intermediate junctions;

a programmable non-volatile memory that stores at least one digital gamma value;

select logic, coupled to said memory and to said plurality of potentiometers, that selects from among said plurality of intermediate junctions for inserting said plurality of potentiometers and that selects each of said variable tap voltages according to said digital gamma value; and

a plurality of buffers having inputs receiving selected tap voltages and outputs that provide said set of gamma corrected bias voltages.

20. The imaging system of claim 19, wherein said programmable gamma correction voltage generator is incorporated on an IC.

21. The imaging system of claim 19, wherein said imaging device comprises an LCD panel.

22. The imaging system of claim 19, further comprising control logic coupled to said memory via address control, wherein said control logic enables selection of a plurality of digital gamma values stored in said memory.

EVIDENCE APPENDIX

There was no evidence submitted pursuant to 37 C.F.R. §§1.130, 1.131 or 1.132.

RELATED PROCEEDINGS APPENDIX

None.